# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/499,720 | 02/08/2000 | Dale C. Morris | 10991915-1 | 1658 |

| 22879 | 7590 | 10/19/2005 |
|---|---|---|

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

| EXAMINER |
|---|
| ROJAS, MIDYS |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on _28 September 2005_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) _1-24_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-24_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _02 August 2000_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1.     Applicant's arguments with respect to independent claims 1, 6, 12, 17, and 23 have been fully considered but they are not persuasive.

Applicant argues that the Arora patent does not teach nor suggest reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level.    However, Arora discloses comparing the architectural current privilege level (previous privilege.level state) with the privilege level of the EPC instruction (current privilege level state) wherein comparing privilege levels, it is understood that the stored privilege level (stored in CPL 38) must be read in the comparison process.  See Col. 6, lines 46-61.

Applicant also argues that the Arora patent does not disclose the limitation of promoting the current privilege level to a second privilege level which is higher that the first privilege level if the previous privilege level state is equal to the is equal to or less privilege that the current privilege level.   However, Arora discloses increasing the current privilege level if the privilege level of the EPC is higher than the CPL (Col. 6, lines 46-61).

2.  Applicant's other arguments with respect to claims 1, 6, 12, 17, and 23 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 112*

3.  The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5, and 12-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding independent claims 1 and 12, the relationship between the stored previous privilege level and the first privilege level is unclear. It is unclear as to what privilege level is being stored as a previous privilege level.

The examiner would like to suggest amending the claim as follows to overcome this rejection:

Claim 1, line 7, replace "instruction including: reading a stored previous privilege level..." with - - instruction including: storing the first privilege level as a stored previous privilege level state; reading a stored previous privilege level..."

Claim 12, line 9, replace "instruction as follows: reads the previous privilege level..." with - - instruction as follows: stores the first privilege level as a previous privilege level state; reads the previous privilege level..."

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arora (6,393,556) in view of Mattison (US 2002/0069316).

Regarding Claims 1 and 6, Arora discloses a method of promoting a current privilege level ("change current privilege level to a higher privilege level", Column 6, lines 46-61) wherein the current privilege level controls application instruction execution in the system by controlling accessibility to the system resources (Column 1, lines 30-41), the method comprising: performing a privilege level promotion instruction by the operating system (Column 4, lines 13-27, and Column 6, lines 46-61), the privilege promotion instruction being stored in a first page of memory (instruction memory 36 storing a plurality of instructions... see Figure 2) wherein processing these instructions direct the processor to change the privilege level (privilege promotion instructions, see Col. 2, lines 19- 37), the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state (CPL 38) to the current privilege level (comparing the current privilege level to the instructions privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49); and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level...", promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process.

Arora discloses processing "branch" instructions (Col. 3, lines 55-67) and "return" instructions instructing the program to return from a subroutine; wherein branch and return instructions need return addresses for returning from a particular branch. Branch instructions involve altering the program path by branching to a subroutine in a particular branch address and returning to the original program path using a stored return address.

Arora does not teach storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. Mattison discloses restricting processor access to instructions stored in main memory when in a particular mode of operation (in this case main memory is not writable by the processor and this particular mode of operation represents the processor's privilege level, see paragraphs 0015-0016). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to restrict access to memory as done by Mattison thus allowing the system to only allow authorized modifications to memory (Mattison, paragraph 0014).

Regarding Claims 12, 17 and 23 Arora discloses a computer system comprising a processor (Figure 2, processor 30) having current privilege level which controls accessibility to the system resources (Column 1, lines 30-41 and Column 4, lines 13-16; see Figure 2, CPL 38) and having a previous privilege level state ("second privilege level", Column 6, lines 27-32); a memory (Figure 2, Instruction memory 36) having a plurality of memory pages including a first memory page storing a privilege promotion instruction ("memory stores a plurality of instructions" such as an "EPC instruction which

directs the processor to change the privilege level of the architectural current privilege level"; see Column 3, lines 20-25 and Column 4, lines 13-27); and performing the privilege level promotion instruction as follows: reading a stored previous privilege level state; comparing the read previous privilege level state (stored in CPL 38) to the current privilege level (comparing the stored current privilege level to the instructions privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49, column 6, lines 46-49); and if the previous privilege level state (stored in CPL 38) is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level...", promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process.

Arora discloses processing "branch" instructions (Col. 3, lines 55-67) and "return" instructions instructing the program to return from a subroutine; wherein branch and return instructions need return addresses for returning from a particular branch. Branch instructions involve altering the program path by branching to a subroutine in a particular branch address and returning to the original program path using a stored return address.

Arora does not teach storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. Mattison

discloses restricting processor access to instructions stored in main memory when in a particular mode of operation (in this case main memory is not writable by the processor and this particular mode of operation represents the processor's privilege level, see paragraphs 0015-0016). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to restrict access to memory as done by Mattison thus allowing the system to only allow authorized modifications to memory (Mattison, paragraph 0014).

Regarding Claims 2, 8, 13, and 19, Arora discloses the method of promoting a current privilege level wherein the step of performing the privilege promotion instruction further includes: if the previous privilege level state is more privileged then the current privilege level ("if the EPC instruction specifies a privilege level lower than or the same as the architectural current privilege level..."), taking an illegal operation fault ("the processor will issue a fault", Column 6, lines 55-61).

Regarding Claims 3, 9, 14, and 20, Arora discloses the method of promoting a current privilege level wherein the system resources include system registers (architectural register set, Column 3, lines 61-67).

Regarding Claims 4, 10, 15, and 21, Arora discloses the method of promoting a current privilege level wherein the system resources include system instructions ("memory 36 stores a plurality of instructions that are processed in the pipeline", column 3, lines 22-25).

Regarding Claims 5, 11, 16, and 22, Arora discloses the method of promoting a current privilege level wherein the system resources include memory pages (Figure 2, instruction memory 36).

Regarding Claim 7, 18, and 24 Arora discloses the method of promoting a current privilege level further comprising: performing a return instruction including: transferring instruction control flow to the stored return address to the first page of memory ("a return instruction would instruct the processor to decrease the architectural current privilege level to the previous privilege level", Column 6, line 65-Column 7, line 3); and demoting the current privilege level to the stored previous privilege level.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is 571-272-4207. The examiner can normally be reached on M-F 5:30 AM - 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 14th, 2005

MR

*Nidys Rojas*
ART Unit 2185

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
10/17/05